REMARKS

Applicant will address the Office Action according to the order in which issues were raised therein.

Drawings

The Examiner has objected that the drawings do not include two reference signs: (1) V_{ref} and (2) non-overlapping four phase clock.

In response, Applicant has amended page 13 to indicate that the reference voltage V_{ref} is not shown on the drawing. It is not a reference sign and therefore need not be shown. With respect to the non-overlapping four-phase clock, the Examiner is referred to page 17, lines 7-8, which identifies the four-phase clock as shown in Fig. 9, each phase of which is identified by reference character. It is not seen that there is any need to label the aggregate of Fig. 9 as page 17 already identifies clearly the four-phase clock. Accordingly, no drawing corrections are necessary. If the Examiner believes otherwise, he is requested to explain with particularity the amendment to the drawings necessary to achieve compliance with 37 C.F.R. §1.84(p)(5).

Formal drawings are submitted herewith. Applicant notes that in preparing the formal drawings, a correction has been made on Fig. 10, shown in a copy marked in red. Switch "S19" should have been Switch "S17," consistent with the labeling of that switch in other figures.

Claim Rejections – 35 U.S.C. §1.12, First Paragraph

Claims 1-9, 16-24, 27-29 and 31-40 have been rejected under 35 U.S.C. §112, first paragraph, as not being enabled by the specification. The Examiner then lists a number of points with respect to things he does not understand in the specification. However, he never relates them to the claimed subject matter. Accordingly, this rejection is improper in form and content. Applicant will attempt to address the issues raised by the Examiner and to clarify his understanding, but without a clear rejection explaining why a given claim is not enabled, Applicant does not know what portion of the specification the Examiner has looked to for support of a given claim element. Thus, the Office Action really does not afford Applicant's a

proper basis for understanding the rejection or for providing the Examiner with the kind of response he requires. All claims are, indeed, properly enabled by the specification.

Under Paragraph 5(a), the Examiner indicates that he does not understand how the switched capacitor, the sub-DACs, elements QDAC1 to QDACN and the charge sharing network in Fig. 4 are interconnected with each other since the interconnecting relationship is not described in the specification as well as is shown in any drawings of the present invention. It may help to point out to the Examiner that the notations Q_{DAC1}... Q_{DACN} relate not to elements but to the charges (Q being the conventional symbol for charge) for each of the respective sub-DACs. As stated on page 12, the DAC 150 comprises four switched capacitor DACs, sometimes referred to as sub-DACs. The text goes on to explain that a first one of the sub-DACs has a reference voltage connected to a first terminal of the switch, etc. On page 12, at lines 4-5, it is expressly stated that each of the sub-DACs shares charge via a charge sharing network with at least one other of the sub-DACs. The details as to how that charge sharing occur in a specific embodiment are specified at, for example, page 12, line 15-page 14, line 32. Other embodiments are discussed in connection with Figs. 8A-8D, commencing on page 16, at line 15, and elsewhere in connection with other figures. Accordingly, the interconnection and charge sharing of the sub-DACs is extensively described. Indeed, it is described in greater detail than is required for one skilled in the art to understand the invention and how it may be practiced.

In Item 5(b), the Examiner expresses that "it is not understood what the signal waveform P1 + P2 in Fig. 5 of the present invention really is since it is not shown in the drawings of the present invention." The Examiner's puzzlement is now, finally, understandable. The specification on page 13 has been amended in a way that should resolve that puzzlement. The specification is more closely conformed to Fig. 5. The specification now makes clear that Switch S13 is controlled by the P1 + P2 signal, which is the logical-ORing of the P1 and P2 signals. Any knowledgeable electriconics engineer will understand the waveform resulting from logically-ORing signals P1 and P2.

With respect to item 5(c), the Examiner has correctly identified a discrepancy between the text on page 29 and Figs. 28A-B. Accordingly, the text on page 29 is amended to change "P2" to "P3." This conforms the text and drawings.

In item 5(d), the Examiner indicates a lack of understanding of the equations in a number of figures because the label "V_{ref}" is not shown in those drawings. As explained above, V_{ref} is not a label, but, rather, a value. Accordingly, there is no basis for requiring a label in the drawings.

In item 5(e), the Examiner indicates a lack of understanding about three labels in Fig. 30 "since they are not really described in the specification." In the formal drawing, the labels "selectable gain" and "external cap" are deleted and lead lines are provided for the legend "voltage output."

It will be readily understood from the specification that the circuit of Fig. 30 has a voltage output.

In item 5(f), the Examiner states "it is not understood how each of the switches 202, 204, 206, 208, S4, S49 and S50 in Fig. 15 is having one open terminal." The Examiner's statement is not understandable. Elements 202-208 are not switches but, instead, are one-bit DACs. See, for example, page 19, line 13. S4 (see Fig. 5) has both terminals connected. One terminal is connected to a voltage V_3 and the other is connected to one terminal of each of switches S5 and S6. In Fig. 15, switches S49 and S50 are shown as having one open terminal because the description of the invention does not depend upon what is connected to the other terminal of the switch. As stated, on page 20, lines 23-25, for example, "in one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47." That is, the other terminal of each of those switches is not intended to be connected. The switch is functioning as a capacitance, not as a switching element.

A similar point is raised by the Examiner in item 5(g) and Applicant's response is similar.

In item 5(h), the Examiner indicates a lack of understanding of the label "NC" in several figures, since it is not described in the specification. This label, meaning "no connection," has been deleted from the formal drawings.

In item 5(i), the Examiner indicates "it is not understood what the four arrows on the right-side of scrambler 400 in Fig. 24 really are since they are not described in the specification." Those arrows will inherently be understood as the output of the scrambler 400. It is not seen that

there is any need to attach a label to those arrows or to expressly make the statement, in the specification, that they are the scrambler's output. If the Examiner believes such labeling is necessary, Applicant would entertain the suggestion of an amendment from the Examiner.

In item 5(j), the Office Action states

> it is not understood what P1 + bit 1.P2, P1 +bit2.P2, P1 + bit 3.P2 and P1 + bit4.P2 in Fig. 31 really are and how they are generated since they are not described in the specification and their signal waveforms are not shown in the drawings of the present invention.

The Examiner's concern is unjustified and the nature of what he does not understand is not at all clear. Applicants must presume that the Examiner understands Boolean expressions. For example, P1 + bit1.P2 means that the value of bit 1 is logically "AND-ed" with the P2 signal value and the result of that AND operation is then "ORed" with the P1 signal. Any electrical engineering graduate would be able to draw the waveform that results from this logical operation, given waveforms for P1 and P2. Therefore, providing the Boolean expression is equivalent to providing the waveform. The Examiner is thus without justification for requiring that the waveforms be drawn expressly, assuming that is what he is asking for. If the Examiner is taking the position that the Boolean algebra is not understood, Applicants would be happy to supply excerpts from any number of text books, but it not seen at this time that the same should be required. Reconsideration is therefore requested.

Claim Rejections – 35 U.S.C. §103

Claims 1-9 and 34-37 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Fling et al., in view of Mehta et al. Essentially, this is a repetition of a prior rejection to which Applicant has provided a full response in its Amendment of June 10, 2003. However, the Examiner either misses essential claim limitations or mischaracterizes or misunderstands Fling '832. Moreover, although the Office Action lists claim 34 as being subject to this rejection, this is believed to be a mistake since claim 34 depends from claim 33, which is not covered by this rejection. Therefore, claim 34 is addressed separately in conjunction with the rejection of claim 33. Applicants respectfully traverse these rejections.

a. The Combination is Improper

First, no motivation is provided in the Office Action from the prior art (whether the cited references or otherwise) to make the proposed combination. In order to establish a *prima facie* case of obviousness, there must be some suggestion or motivation in the prior art to make the proposed combination. The Examiner appears to be using the Applicants' own specification as the motivation for the proposed combination; such a use of hindsight is improper. The Office Action has provided no motivation for the proposed combination in either Fling or Mehta or any other references. Such motivation would not have existed. Fling is directed to a system for processing the video information in a video signal (col. 1, lines 10-26). In order to enhance the image quality of certain digital video receivers, Fling attempts to double the number of horizontal lines displayed per frame while keeping the frame rate constant (col. 1, lines 27-35). This is because a television rasters the image onto the screen many times a second. Thus, video data is inherently serial; there is no need for a multi-bit DAC in the device of Fling, because Fling attempts to solve a problem which is inherently single bit. Not only would those skilled in the art have perceived no motivation to make the combination, but also it makes no sense to combine the multi-bit signal of Mehta with the device of Fling and/or other references. Therefore, the rejection under 35 U.S.C. 103(a) over the combination of Fling and Mehta is improper where the use of a multi-bit signal would be inappropriate to Fling's intended use. The rejection should be withdrawn.

b. Applicants' Claims Distinguish Over the Proposed Combination

Even assuming *arguendo* that the proposed combination of Fling, Mehta, etc. did make sense and further assuming there was some hypothetical motivation, the proposed combination would still not meet and make obvious claims 1-9 and 34-37of the present invention.

If one were to combine the teachings of Fling and Mehta, without reaching the tertiary references, one can posit that the resulting device would use the ping-pong DACs of Fling and the multi-bit digital input of Mehta, as suggested on page 5 of the Office Action. Each bit of the multi-bit signal would enter a pair of pin-ponged DACs and would be converted to an analog

signal at twice the rate as would be accomplished with only one of the DACs. However, such a device would neither anticipate nor make obvious any of claims 1-9 or 34-37, because, contrary to the assertion of the Office Action, Fling does not disclose a system having a DAC that receives a multi-bit digital signal and outputs *at least two* analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of the *same bits* in the multi-bit digital signal.

Firstly, Fling discloses only a DAC system having inside it **two** DACs (elements 16 and 18), **each of which output a *single* analog signal** (col. 2, lines 49-58). In contrast, claim 1 recites a system having **a DAC (i.e., a single DAC, not two) that receives a multi-bit digital signal and outputs at least *two* analog signals (i.e., one DAC, two output signals).** Secondly, those output signals include a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal and the second analog signal also being indicative of ***the same*** sum of values of said bits in the multi-bit digital signal. By contrast, each of Fling's ping-ponged DACs operate on ***different*** input bits and produces a *single* output. Neither of the DACs making up the DAC converter system of Fling, even when modified by Mehta to take in a multi-bit signal, outputs at least two analog signals, with or without the other two references, much less the claimed signals. Therefore, claim 1 is unobvious and patentably distinguishes over the combination of Fling and Mehta, and Applicants respectfully request that the rejection of claims 1-9 and 34-37 be withdrawn.

In addition, thirdly, nowhere in Fling or Mehta is it taught or suggested that the single analog value output by each of DACs 18 and 16 is indicative of a sum of bits. To the contrary, Fling shows, in Figs. 1 and 2, that the output of each DAC is a sample of *every other* value x_n, where x_n is the value of the single bit signal x at time n. In other words, DAC 16 outputs a series of values x_{n-2}, x_n, x_{n+2}, etc., while DAC 18 outputs a series of values x_{n-3}, x_{n-1}, x_{n+1}, etc. In no way do *each* of DACs 18 and 16 of Fling output **two** analog signals **which are indicative of a sum of bits**. Even the output 25 of the sum of the signals 20 and 22 is not indicative of a sum of bits; instead, it is indicative of an analog version of the time-varying single-bit signal 10. Signals

20 and 22 are out-of-phase samples of the same, single-bit signal which combine to produce not two summed signals, but an analog version of the original signal.

Ignoring the fact that there is no demonstrated motivation to combine the pin-pong video converting DACs of Fling with the multi-bit sound signals of Mehta, if one of ordinary skill in the art were asked to combine the two by using one of Fling's one-bit ping-pong DAC systems for each bit of the multi-bit system, such a system would still not meet the claims of the present invention because 1) there would be no DAC that could output two analog signals, and 2) there would be no DAC which could output two analog signal indicative of a sum of values of bits, since each pin-pong DAC pair takes in a single-bit signal.

In contrast, claim 4, the second independent claim, recites a method comprising receiving a multi-bit digital signal and generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of ***"said"*** sum of values of said bits in the multi-bit digital signal.

As discussed above, nowhere in Fling or Mehta, or the other references, is it disclosed to generate at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of the ***same*** sum of values of the same bits in the multi-bit digital signal.

Similarly, claim 7 recites a system comprising means for receiving a multi-bit digital signal and means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

Thus, for the reasons cited above, claims 1-9 and 35-37 patentably distinguish over, and are not obvious in light of, the proposed combination of Fling and Mehta. Consequently, the rejection of these claims under 35 U.S.C. §103(a) should be withdrawn.

2. Claim 27 is patentable.

The Office Action incorrectly maintains a rejection of claim 27 as obvious over Yamashita (U.S. Patent No. 5,890,432) in view of Dingwall et al. (U.S. Patent No. 5,332,997).

The Office Action states that Yamashita shows (citing FIG. 4) a handset that includes a digital to analog converter 307, and that Dingwall discloses a switched capacitor DAC network comprising a plurality of DACs 11 (citing FIG. 6) each of which comprises a plurality of capacitors that share charge with one another (citing FIG. 2).

The Office Action further states that Yamashita does not show a switched capacitor network having a plurality of DACs as recited in claim 27, but that it would have been obvious to utilize the switched capacitor DAC network in FIGS. 2, 6 of Dingwall for the DAC 307 in FIG. 4 of Yamashita, for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al., "for the purpose of loading data at a high speed").

1. The proposed combination is improper.

As previously explained **and as apparently conceded by the Examiner since he does not contest the point,** and as further discussed below, the proposed combination is improper for at least the following reasons: (1) the references teach away from the proposed combination, (2) the proposed combination would leave the circuit of Yamashita inoperative, and (3) even if the proposed combination would be operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation, which is in fact illusory.

Yamashita discloses a handset in which speech signals are received from a microphone 106, coded by a speech codec 304 and a channel codec 305, and then modulated by a modem 306 to produces modulated in-phase (I) and quadrature-phase (Q) transmitting signals. A DAC 307 converts the modulated in-phase (I) and quadrature-phase (Q) transmitting signals to analog transmitting signals TxDI and TxDQ, respectively, that are transferred to the RF transmitter 202 of the system. (Column 5, lines 34-40).

Dingwall discloses (in FIG. 6), a serial data generator with 40 output data word lines (DWL1 through DWL40). Each output data word line carries 144 bits of serial information which are distributed onto 24 sub lines. Each sub line carries 6 digital data bits to a corresponding serial-input, binary weighted DAC 11, which converts the 6 serial data bits into an

analog signal (col. 5, lines 5-15). The DAC 11 uses a binary weighted capacitive network 50, which is comprised of binary-weighted storage capacitors (FIG. 2, col. 5, lines 58-65).

First, observe that Dingwall itself **teaches away** from the proposed combination. Dingwall states that there are "*problems*" with the DAC shown in FIGS. 2, 6 (see col. 12, lines 15-22). Dingwall states that the binary weighted capacitive network used in the DAC of FIGS. 2, 6 and shown in FIG. 2, requires "*very large*" or "*very small*" capacitors (col. 12, lines 15-22) (emphasis added). The very small capacitors are "*difficult to make accurately*" and there is the "*additional problem*" of stray capacitance (col. 12, lines 22-24) (emphasis added). On the other hand, large capacitors take "*too much space*" (col. 12, lines 23-25) (emphasis added). The "*problem becomes worse*" when more than 6 binary steps are desired (col. 12, lines 21-22) (emphasis added). Dingwall suggests that the problems "may be alleviated" by adding additional circuitry; however, in view of all of these problems, why would anyone skilled in the art even consider using the DAC of Dingwall in the handset of Yamashita? He all but expressly says not to! The Office Action fails to address this highly persuasive point, as previously noted. Instead, it relies on a speculative hindsight effort to pick and choose the features and qualities of the references to be combined. This is improper.

Second, the proposed combination would leave the circuit in Yamashita *inoperative*. The DAC 11 in Dingwall is a serial-input DAC. In contrast thereto, the DAC 307 of Yamashita is coupled to a channel coder 305 (which typically produce a parallel output), therefore suggesting that it is a parallel-input DAC (extra circuitry would be needed if the DAC 307 were not a parallel-input DAC). A serial-input DAC is not interchangeable with a parallel-input DAC, and therefore, cannot be substituted for the parallel-input DAC 307 of Yamashita, without leaving the circuit inoperative, a result that clearly makes the proposed combination improper. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. Further, even if the circuit of Yamashita could be further modified (by adding additional circuitry not proposed by the Office Action) so as to operate with the DAC of Dingwall, such modifications have not been proposed by the Office Action, and the potential impact to size, cost, power, performance, etc., clearly teaches away from any attempts to do so.

The Office Action states that one skilled in the art would carry out the proposed modification for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al.). This proposed motivation is *illusory* and is an improper effort to find motivation where there is none. *Firstly, one skilled in the art would not make a modification that would leave the circuit unusable for its intended purpose*! Secondly, even if the proposed combination were operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation.

To try to satisfy the Office's burden of proof as to motivation, the Office Action cites a statement from Dingwall to the effect that data is loaded very quickly onto the gates of the switching transistors. The Office Action thus implies that one skilled in the art would make the modification to improve speed. However, the "evidence" set forth by the Office Action merely implies that the DAC in Dingwall may be faster than other *Dingwall-type* DACs. This says absolutely *nothing* about whether there is a speed advantage to putting the DAC of Dingwall into Yamashita, and is thus factually, logically and legally *irrelevant*. If speed is the concern, then the issue is not whether the DAC of Dingwall is faster than other Dingwall type DACs, but rather, the speed of the serial-input DAC in Dingwall compared to the speed of the parallel-input DAC in Yamashita. Yet the evidence set forth by the Office Action does not say anything about the speed of the DAC in Dingwall versus the DAC in Yamashita. Consequently, *there is no support for the contention that the proposed combination, even if operational, would be expected to produce a speed improvement in Yamashita.* Thus, the Office's burden of proof as to motivation is not met.

Moreover, because the DAC of Dingwall is a serial-input DAC and the DAC in Yamashita would appear to be a parallel-input DAC, it is likely that the DAC of Dingwall is actually *slower*, not faster, than the DAC in Yamashita, thereby actually teaching *away* from the proposed combination.

Consequently, the proposed combination is improper and neither Yamashita, nor Dingwall nor any legally tenable combination thereof, teaches or suggests the inventions recited in claim 27.

F. Rejections Under 35 U.S.C. §102

Paragraph 8 of the Office Action rejects claims 17-24, 28-33 and 38-40 under 35 U.S.C. §102(e) as being anticipated by Watson et al., 6,154,162. (Applicants wish to point out that there is no claim 28 pending in this application, and that there is also a claim 41 which has not been addressed but which depends from rejected claim 29; Applicants assume herein that the rejection is of claims 17-24, 29-33, and 38-41.) Applicants respectfully traverse this rejection.

1. Prima Facie Insufficiency of the Rejection

This rejection, unfortunately, is insufficient on its face, to a degree that the Action should be withdrawn and a new one issued. Among the rejected claims there are at least *three dozen* elements and limitations. The exposition of the rejection in paragraph 8 is less than three lines long, identifying in Watson only scrambler 42, SC DAC 32, capacitors 70, 72, and 74, and an unsupported assertion that the capacitors share charge. Applicants are left to speculate where the Examiner believed he may have found all of the *other* claim elements and limitations. Both under 37 C.F.R. 1.104(c)(2) and the corresponding MPEP mandate to explain the rejection in sufficient detail to permit consideration and response by Applicants, this rejection fails to meet the requirements. Accordingly, no response is required.

Nevertheless, to advance prosecution, Applicants will distinguish Watson.

2. Discussion of Watson

Watson is directed to a digital-to-analog converter (DAC) which uses switched capacitors summed to an op amp to generate an analog voltage (Abstract). Watson makes use of a thermometer encoder to reduce the size of capacitors used, and thus reduce the error in the capacitor (col. 4, lines 20-32). Watson makes use of a scrambler to further reduce the dependency of the error on a select few of the capacitors (col. 4, lines39-50). Only the higher order bits are scrambled in order to reduce complexity and cost (col. 4, lines 51-56).

3. Applicants' Claims Distinguish Over Watson

The Office Action states in its rejection that Watson discloses in Fig. 4 a digital signal processing system comprising: scrambler 42, switched capacitor DAC 32 including a plurality of capacitors 70, 72, and 74 *sharing charge with one another*. Applicants respectfully disagree. The Examiner has misunderstood Watson. Claim 17 is directed to "a system having a digital signal processing stage comprising a scrambler that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC having a plurality of sub-DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC *having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed*, and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC using less than all of the redistributed charge."

Quite simply, nowhere does Watson disclose a device in which at least two of the plurality of sub-DACs share charge with one another such that the associated charges are redistributed (i.e., between capacitors).

Referring to Fig. 4 of Watson, each of the capacitors 70, 72, and 74 referenced by the Office Action correspond to the sub-DACs of claim 17. However, these capacitors are connected through a node which is forced to maintain a specific voltage. Watson discloses that when switches 78 are connecting capacitors 70, 72, and 74 to Vref or ground, switch 68 connects node 58 to a constant voltage VCM (col. 6, lines 43-45). Watson states, "Thus, both sides of capacitors 70, 72, 74, and linking capacitor 50 are driven to constant voltages, allowing the capacitors to be fully charged or discharged." (col. 6, lines 45-48). **Since both terminals of every sub-DAC capacitor of Watson are driven to a constant voltage, there can be no charge sharing of charge with one another such the associated charges are redistributed.** This is almost as explicit a teaching away from the claimed invention as one could imagine finding.

Watson does disclose that in the summing phase of operation, the charge of the subDAC capacitors 70, 72, and 74 is discharged from the summing node 58 into the bypass capacitor 60 (col. 6, lines 52-60). However, this does not constitute charge sharing between the subDAC capacitors, since the charge on any subDAC capacitor 70, 72, or 74 cannot affect the charge on any other capacitor.

For at least the foregoing reasons, claim 17 distinguishes over Watson, and the rejection of claim 17 under 35 U.S.C. §102(e) as being anticipated by Watson must be withdrawn.

Claims 18-21 depend from and further limit claim 17, and are believed to be allowable based on their dependency.

Claim 29 likewise recites, inter alia, "the switched capacitor DAC **having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed.**"

For the same reasons discussed above in connection with claim 17, therefore, claim 29 patentably distinguishes over Watson.

Claims 32 and 39-41 depend from claim 29, and are believed to be allowable based on their dependency.

Claim 22 is directed to a digital-to-analog converter that receives a multi-bit digital signal and produces an analog output that is **proportional to the square of the multi-bit digital signal**.

The Office Action has failed to specifically address the limitations of claim 22 with respect to the rejection under 35 U.S.C. §102(e), instead choosing to blindly group it with claim 17, which is not at all similar. Nonetheless, as is obvious, nowhere does Watson disclose a DAC that receives a multi-bit digital signal and produces an analog output that is **proportional to the square of the multi-bit digital signal**.

Therefore, claim 22 patentably also distinguishes over Watson, and its rejection must be withdrawn.

Claims 23-24 depend from claim 22, and are allowable for at least the same reasons.

Claim 33 is directed to a system comprising: a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC wherein

the DAC comprises a switched capacitor network that receives a multi-bit input that includes the multi-bit output from the digital signal processing stage, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, **the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another**, and having an operating state in which less than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit input received by the DAC.

For at least the reasons discussed above in connection with claims 17 and 29, claim 33 patentably distinguishes over Watson. Namely, nowhere does Watson teach or disclose a DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another. Therefore, the rejection of claim 33 as being anticipated by Watson should be withdrawn.

Claim 34 depends from claim 33, and is allowable for at least the same reasons.

Claim 38 was rejected under 35 U.S.C. §102(e) over Watson; however, claim 38 depends from claim 1, which has been rejected under 35 U.S.C. §103 in the same Office Action. Since claim 1 is believed to have been placed in condition for allowance previously in this response and has not been rejected under 35 U.S.C. §102(e) over Watson, Applicants do not address the rejection of claim 38, as it is believed to be allowable based on its dependency. However, Applicants reserve the right to make such an argument in the future.

G. Provisional Double Patenting Rejection

Paragraph 10 of the Office Action states that claims 1-9 and 34-37 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-17 of copending Applicant No. 09/575,561.

Applicants note that this rejection is provisional and therefore does not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

The rejections under 35 U.S.C. §102 and 103 track rejections previously made by the Examiner and Applicants' response tracks Applicants' previous response because it is apparent from the record that for procedural or other reasons the Examiner has not substantively considered Applicants' previous response. Full consideration at this time is requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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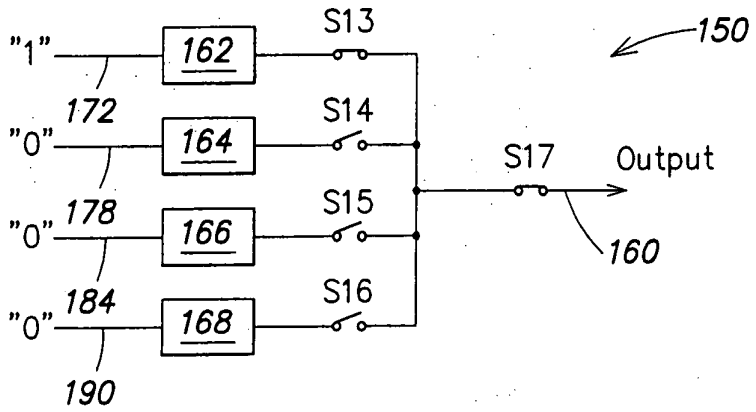
Docket No.: A0312.70409US00
Date: March 3, 2004
x03/10/04



P1 = "0"	$V(C1) = V_{ref}/4$	$Q(C1) = C*V_{ref}/4$
P2 = "1"	$V(C2) = V_{ref}/4$	$Q(C2) = C*V_{ref}/4$
P3 = "0"	$V(C3) = V_{ref}/4$	$Q(C3) = C*V_{ref}/4$
	$V(C4) = V_{ref}/4$	$Q(C4) = C*V_{ref}/4$

FIG. 7C

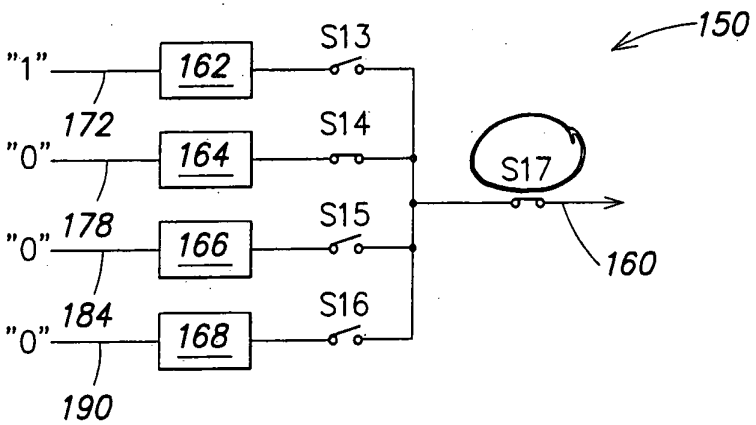


FIG. 10

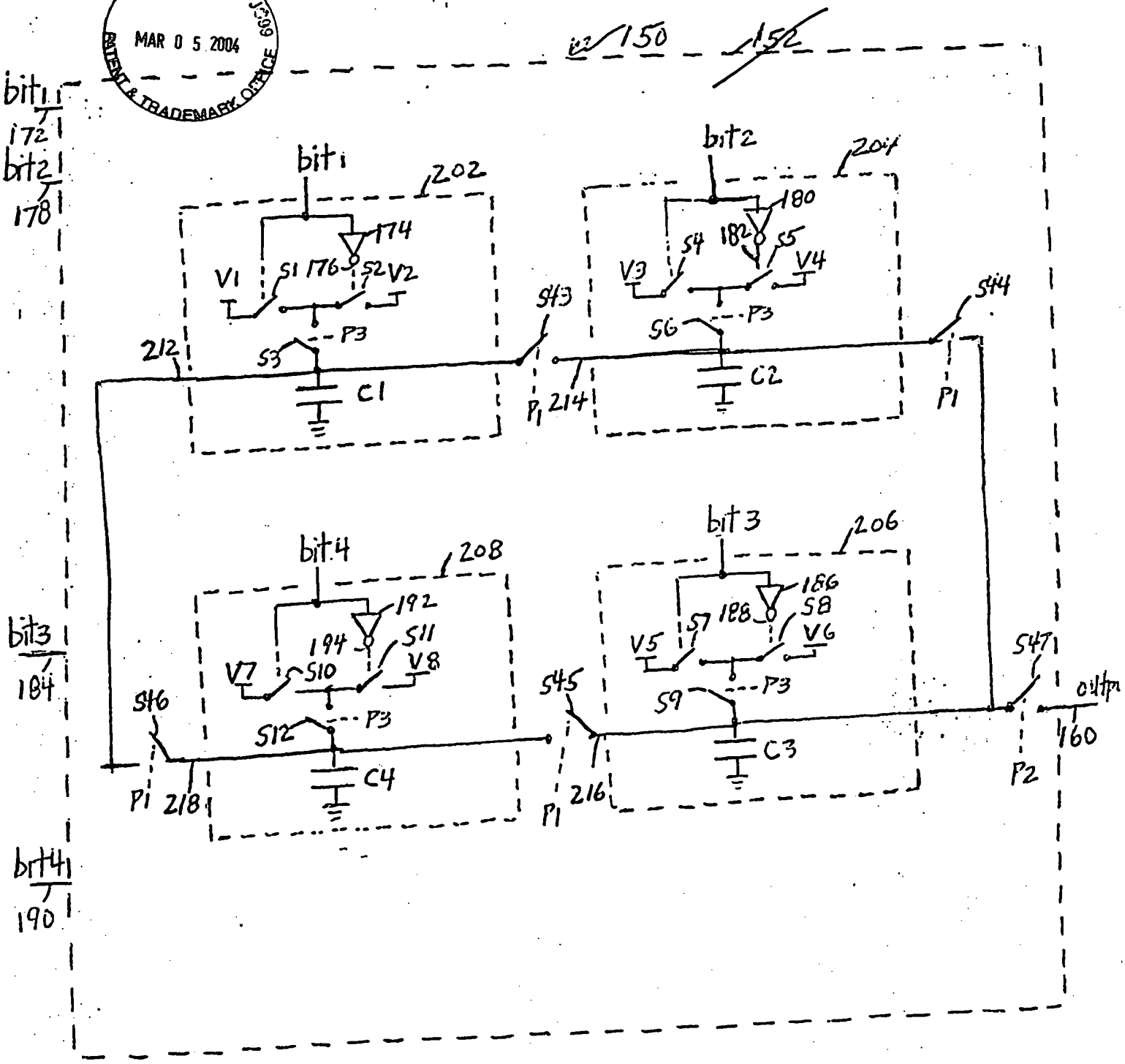


FIG. 13